ELPIDA

DATA SHEET

256MB, 512MB Registered DDR SDRAM DIMM

HB54A2569F1 (32M words × 72 bits, 1 Bank)
HB54A5129F2 (64M words × 72 bits, 2 Banks)

Description

The HB54A2569F1, HB54A5129F2 are Double Data Rate (DDR) SDRAM Module, mounted 256M bits DDR SDRAM (HM5425801BTT) sealed in TSOP package, 1 piece of PLL clock driver, 2 pieces of register driver and 1 piece of serial EEPROM (2k bits EEPROM) for Presence Detect (PD).

The HB54A2569F1 is organized as 32M × 72 × 1 bank mounted 9 pieces of 256M bits DDR SDRAM. The HB54A5129F2 is organized as 32M × 72 × 2 banks mounted 18 pieces of 256M bits DDR SDRAM. Read and write operations are performed at the cross points of the CK and the /CK. This high-speed data transfer is realized by the 2 bits prefetch-pipelined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DLL) can be set enable or disable. An outline of the products is 184-pin socket type package (dual lead out). Therefore, it makes high density mounting possible without surface mount technology. It provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

Features

- 184-pin socket type package (dual lead out)
  - Outline: 133.35mm (Length) × 43.18mm (Height) × 4.00mm (Thickness)
  - Lead pitch: 1.27mm
- 2.5V power supply (VCC/VCCQ)
- SSTL-2 interface for all inputs and outputs
- Clock frequency: 143MHz/133MHz/125MHz (max.)
- Data inputs, outputs and DM are synchronized with DQS
- 4 banks can operate simultaneously and independently (Component)
- Burst read/write operation
- Programmable burst length: 2, 4, 8
  - Burst read stop capability
- Programmable burst sequence
  - Sequential
  - Interleave
- Start addressing capability
  - Even and Odd
- Programmable /CAS latency (CL): 3, 3.5
- 8192 refresh cycles: 7.8µs (8192/64ms)
- 2 variations of refresh
  - Auto refresh
  - Self refresh

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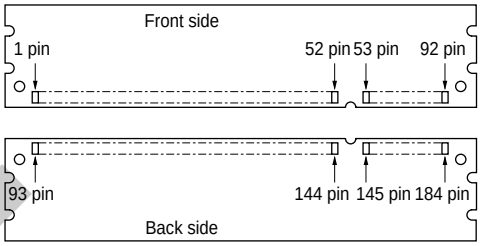
Ordering Information

Part number	Clock frequency MHz (max.)	/CAS latency	Package	Contact pad
HB54A2569F1-A75B*[1]	133	3.0	184-pin dual lead out socket type	Gold
HB54A2569F1-B75B*[2]	133	3.5		
HB54A2569F1-10B*[3]	100	3.0		
HB54A5129F2-A75B*[1]	133	3.0		
HB54A5129F2-B75B*[2]	133	3.5		
HB54A5129F2-10B*[3]	100	3.0		

Notes: 1. 143MHz operation at /CAS latency = 3.5.
2. 100MHz operation at /CAS latency = 3.0.
3. 125MHz operation at /CAS latency = 3.5.

Pin Configurations



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREF	47	DQS8	93	VSS	139	VSS
2	DQ0	48	A0	94	DQ4	140	DM8/DQS17
3	VSS	49	CB2	95	DQ5	141	A10
4	DQ1	50	VSS	96	VCCQ	142	CB6
5	DQS0	51	CB3	97	DM0/DQS9	143	VCCQ
6	DQ2	52	BA1	98	DQ6	144	CB7
7	VCC	53	DQ32	99	DQ7	145	VSS
8	DQ3	54	VCCQ	100	VSS	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	/RESET	56	DQS4	102	NC	148	VCC
11	VSS	57	DQ34	103	NC	149	DM4/DQS13
12	DQ8	58	VSS	104	VCCQ	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	VSS
15	VCCQ	61	DQ40	107	DM1/DQS10	153	DQ44
16	NC	62	VCCQ	108	VCC	154	/RAS
17	NC	63	/WE	109	DQ14	155	DQ45
18	VSS	64	DQ41	110	DQ15	156	VCCQ
19	DQ10	65	/CAS	111	CKE1 (NC)*[1]	157	/S0
20	DQ11	66	VSS	112	VCCQ	158	/S1 (NC)*[1]
21	CKE0	67	DQS5	113	NC	159	DM5/DQS14
22	VCCQ	68	DQ42	114	DQ20	160	VSS
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	VCC	116	VSS	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	VSS	72	DQ48	118	A11	164	VCCQ

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
27	A9	73	DQ49	119	DM2/DQS11	165	DQ52
28	DQ18	74	VSS	120	VCC	166	DQ53
29	A7	75	NC	121	DQ22	167	NC
30	VCCQ	76	NC	122	A8	168	VCC
31	DQ19	77	VCCQ	123	DQ23	169	DM6/DQS15
32	A5	78	DQS6	124	VSS	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	VSS	80	DQ51	126	DQ28	172	VCCQ
35	DQ25	81	VSS	127	DQ29	173	NC
36	DQS3	82	VCCID	128	VCCQ	174	DQ60
37	A4	83	DQ56	129	DM3/DQS12	175	DQ61
38	VCC	84	DQ57	130	A3	176	VSS
39	DQ26	85	VCC	131	DQ30	177	DM7/DQS16
40	DQ27	86	DQS7	132	VSS	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	VSS	88	DQ59	134	CB4	180	VCCQ
43	A1	89	VSS	135	CB5	181	SA0
44	CB0	90	NC	136	VCCQ	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	VCC	92	SCL	138	/CK0	184	VCCSPD

Note: 1. The HB54A2569F1 assign “NC”.

Pin Description

Pin name	Function
A0 to A12	Address input Row address A0 to A12 Column address A0 to A9
BA0, BA1	Bank select address
DQ0 to DQ63	Data input/output
CB0 to CB7	Check bit (Data input/output)
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
/S0, /S1	Chip select
CKE0, CKE1	Clock enable
CK0	Clock input
/CK0	Differential clock input
DQS0 to DQS8	Input and output data strobe
DM0 to DM8/DQS9 to DQS17	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SA0 to SA2	Serial address input
VCC	Power for internal circuit
VCCQ	Power for DQ circuit
VCCSPD	Power for serial EEPROM
VREF	Input reference voltage
VSS	Ground
VCCID	VCC identification flag
/RESET	Reset pin (forces register inputs low)
NC	No connection

Serial PD Matrix*[1]

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes utilized by module manufacturer	1	0	0	0	0	0	0	0	80H	128
1	Total number of bytes in serial PD device	0	0	0	0	1	0	0	0	08H	256 bytes
2	Memory type	0	0	0	0	0	1	1	1	07H	SDRAM DDR
3	Number of row address	0	0	0	0	1	1	0	1	0DH	13
4	Number of column address	0	0	0	0	1	0	1	0	0AH	10
5	Number of DIMM banks HB54A2569F1	0	0	0	0	0	0	0	1	01H	1
	HB54A5129F2	0	0	0	0	0	0	1	0	02H	2
6	Module data width	0	1	0	0	1	0	0	0	48H	72 bits
7	Module data width continuation	0	0	0	0	0	0	0	0	00H	0 (+)
8	Voltage interface level of this assembly	0	0	0	0	0	1	0	0	04H	SSTL 2.5V
9	DDR SDRAM cycle time, CL = X -A75B	0	1	1	1	0	0	0	0	70H	CL = 2.5*[5]
	-B75B	0	1	1	1	0	1	0	1	75H	
	-10B	1	0	0	0	0	0	0	0	80H	
10	SDRAM access from clock (tAC) -A75B, -B75B	0	1	1	1	0	1	0	1	75H	0.75ns*[5]
	-10B	1	0	0	0	0	0	0	0	80H	0.8ns*[5]
11	DIMM configuration type	0	0	0	0	0	0	1	0	02H	ECC
12	Refresh rate/type	1	0	0	0	0	0	1	0	82H	7.8 µs Self refresh
13	Primary SDRAM width	0	0	0	0	1	0	0	0	08H	× 8
14	Error checking SDRAM width	0	0	0	0	1	0	0	0	08H	× 8
15	SDRAM device attributes: Minimum clock delay back-to-back column access	0	0	0	0	0	0	0	1	01H	1 CLK
16	SDRAM device attributes: Burst length supported	0	0	0	0	1	1	1	0	0EH	2, 4, 8
17	SDRAM device attributes: Number of banks on SDRAM device	0	0	0	0	0	1	0	0	04H	4
18	SDRAM device attributes: /CAS latency	0	0	0	0	1	1	0	0	0CH	2, 2.5
19	SDRAM device attributes: /CS latency	0	0	0	0	0	0	0	1	01H	0
20	SDRAM device attributes: /WE latency	0	0	0	0	0	0	1	0	02H	1
21	SDRAM module attributes	0	0	1	0	0	1	1	0	26H	Registered
22	SDRAM device attributes: General	1	1	0	0	0	0	0	0	C0H	± 0.2V
23	Minimum clock cycle time at CLX - 0.5 -A75B	0	1	1	1	0	1	0	1	75H	CL = 2*[5]
	-B75B/10B	1	0	1	0	0	0	0	0	A0H	
24	Maximum data access time (tAC) from clock at CLX - 0.5 -A75B, -B75B	0	1	1	1	0	1	0	1	75H	0.75ns*[5]
	-10B	1	0	0	0	0	0	0	0	80H	0.8ns*[5]
25	Minimum clock cycle time at CLX - 1	0	0	0	0	0	0	0	0	00H	
26	Maximum data access time (tAC) from clock at CLX - 1	0	0	0	0	0	0	0	0	00H	

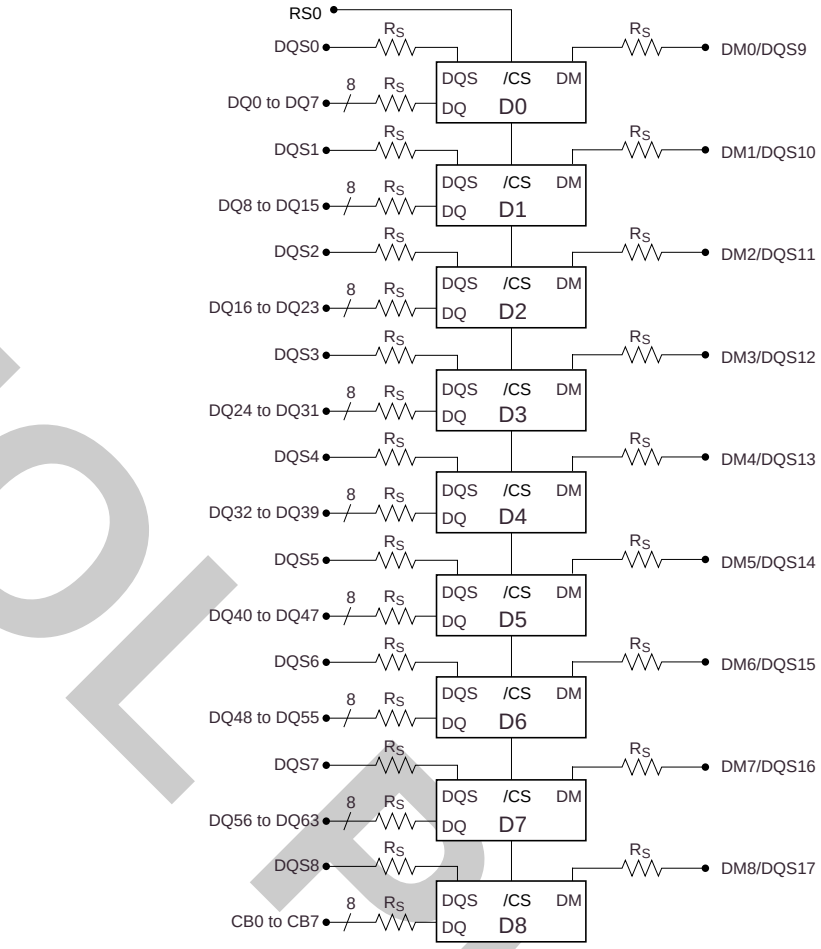
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
27	Minimum row precharge time (tRP)	0	1	0	1	0	0	0	0	50H	20ns
28	Minimum row active to row active delay (tRRD)	0	0	1	1	1	1	0	0	3CH	15ns
29	Minimum /RAS to /CAS delay (tRCD)	0	1	0	1	0	0	0	0	50H	20ns
30	Minimum active to precharge time (tRAS) -A75B, -B75B	0	0	1	0	1	1	0	1	2DH	45ns
	-10B	0	0	1	1	0	0	1	0	32H	50ns
31	Module bank density	0	1	0	0	0	0	0	0	40H	256MB
32	Address and command setup time before clock (tIS) -A75B, -B75B	1	0	0	1	0	0	0	0	90H	0.9ns*5
	-10B	1	0	1	1	0	0	0	0	B0H	1.1ns*5
33	Address and command hold time after clock (tIH) -A75B, -B75B	1	0	0	1	0	0	0	0	90H	0.9ns*5
	-10B	1	0	1	1	0	0	0	0	B0H	1.1ns*5
34	Data input setup time before clock (tDS) -A75B, -B75B	0	1	0	1	0	0	0	0	50H	0.5ns*5
	-10B	0	1	1	0	0	0	0	0	60H	0.6ns*5
35	Data input hold time after clock (tDH) -A75B, -B75B	0	1	0	1	0	0	0	0	50H	0.5ns*5
	-10B	0	1	1	0	0	0	0	0	60H	0.6ns*5
36 to 40	Superset information	0	0	0	0	0	0	0	0	00H	Future use
41	Active command period (tRC) -A75B, -B75B	0	1	0	0	0	0	0	1	41H	65ns*5
	-10B	0	1	0	0	0	1	1	0	46H	70ns*5
42	Auto refresh to active/Auto refresh command cycle (tRFC) -A75B, -B75B	0	1	0	0	1	0	1	1	4BH	75ns*5
	-10B	0	1	0	1	0	0	0	0	50H	80ns*5
43	SDRAM tCK cycle max. (tCK max.)	0	0	1	1	0	0	0	0	30H	12ns*5
44	Dout to DQS skew -A75B, -B75B	0	0	1	1	0	0	1	0	32H	500ps*5
	-10B	0	0	1	1	1	1	0	0	3CH	600ps*5
45	Data hold skew (tQHS) -A75B, -B75B	0	1	1	1	0	1	0	1	75H	750ps*5
	-10B	1	0	1	0	0	0	0	0	A0H	1000ps*5
46 to 61	Superset information	0	0	0	0	0	0	0	0	00H	Future use
62	SPD revision	0	0	0	0	0	0	0	0	00H	Initial
63	Checksum for bytes 0 to 62 HB54A2569F1-A75B	1	1	0	0	1	0	1	0	CAH	202
	HB54A2569F1-B75B	1	1	1	1	1	0	1	0	FAH	250
	HB54A2569F1-10B	1	0	1	1	1	1	1	1	BFH	191
	HB54A5129F2-A75B	1	1	0	0	1	0	1	1	CBH	203
	HB54A5129F2-B75B	1	1	1	1	1	0	1	1	FBH	251
	HB54A5129F2-10B	1	1	0	0	0	0	0	0	C0H	192
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07H	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00H	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	*2 (ASCII-8bit code)

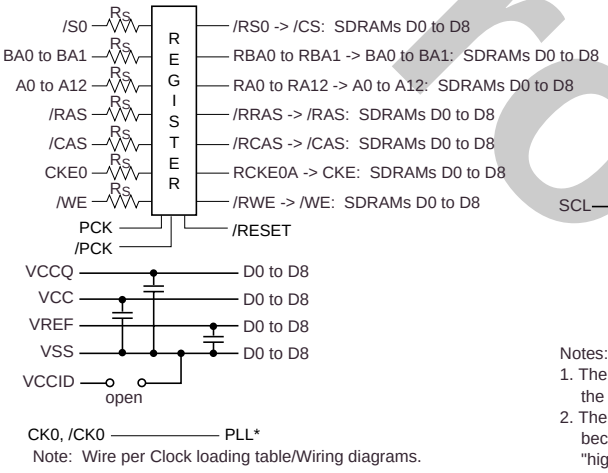
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
73	Module part number	0	1	0	0	1	0	0	0	48H	H
74	Module part number	0	1	0	0	0	0	1	0	42H	B
75	Module part number	0	0	1	1	0	1	0	1	35H	5
76	Module part number	0	0	1	1	0	1	0	0	34H	4
77	Module part number	0	1	0	0	0	0	0	1	41H	A
78	Module part number HB54A2569F1	0	0	1	1	0	0	1	0	32H	2
	HB54A5129F2	0	0	1	1	0	1	0	1	35H	5
79	Module part number HB54A2569F1	0	0	1	1	0	1	0	1	35H	5
	HB54A5129F2	0	0	1	1	0	0	0	1	31H	1
80	Module part number HB54A2459F1	0	0	1	1	0	1	1	0	36H	6
	HB54A5129F2	0	0	1	1	0	0	1	0	32H	2
81	Module part number	0	0	1	1	1	0	0	1	39H	9
82	Module part number	0	1	0	0	0	1	1	0	46H	F
83	Module part number HB54A2569F1	0	0	1	1	0	0	0	1	31H	1
	HB54A5129F2	0	0	1	1	0	0	1	0	32H	2
84	Module part number	0	0	1	0	1	1	0	1	2DH	—
85	Module part number -A75B	0	1	0	0	0	0	0	1	41H	A
	-B75B	0	1	0	0	0	0	1	0	42H	B
	-10B	0	0	1	1	0	0	0	1	31H	1
86	Module part number -A75B, -B75B	0	0	1	1	0	1	1	1	37H	7
	-10B	0	0	1	1	0	0	0	0	30H	0
87	Module part number -A75B, -B75B	0	0	1	1	0	1	0	1	35H	5
	-10B	0	1	0	0	0	0	1	0	42H	B
88	Module part number -A75BB, -B75B	0	1	0	0	0	0	1	0	42H	B
	-10B	0	0	1	0	0	0	0	0	20H	(Space)
89 to 90	Module part number	0	0	1	0	0	0	0	0	20H	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30H	Initial
92	Revision code	0	0	1	0	0	0	0	0	20H	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (BCD)
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (BCD)
95 to 98	Module serial number	*3									
99 to 127	Manufacturer specific data	*4									

Notes: 1. All serial PD data are not protected. 0: Serial data, “driven Low”, 1: Serial data, “driven High” These SPD are based on JEDEC Committee Ballot JC-42.5-99-129.

2. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4AH. 4AH shows “J” on ASCII code.)
3. Bytes 95 through 98 are assembly serial number.
4. All bits of 99 through 127 are not defined (“1” or “0”).
5. These specifications are defined based on component specification, not module.

Block Diagram (HB54A2569F1)

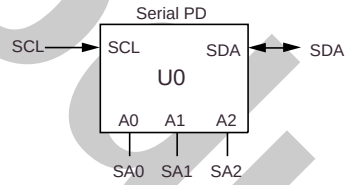




CK0, /CK0 ——— PLL*

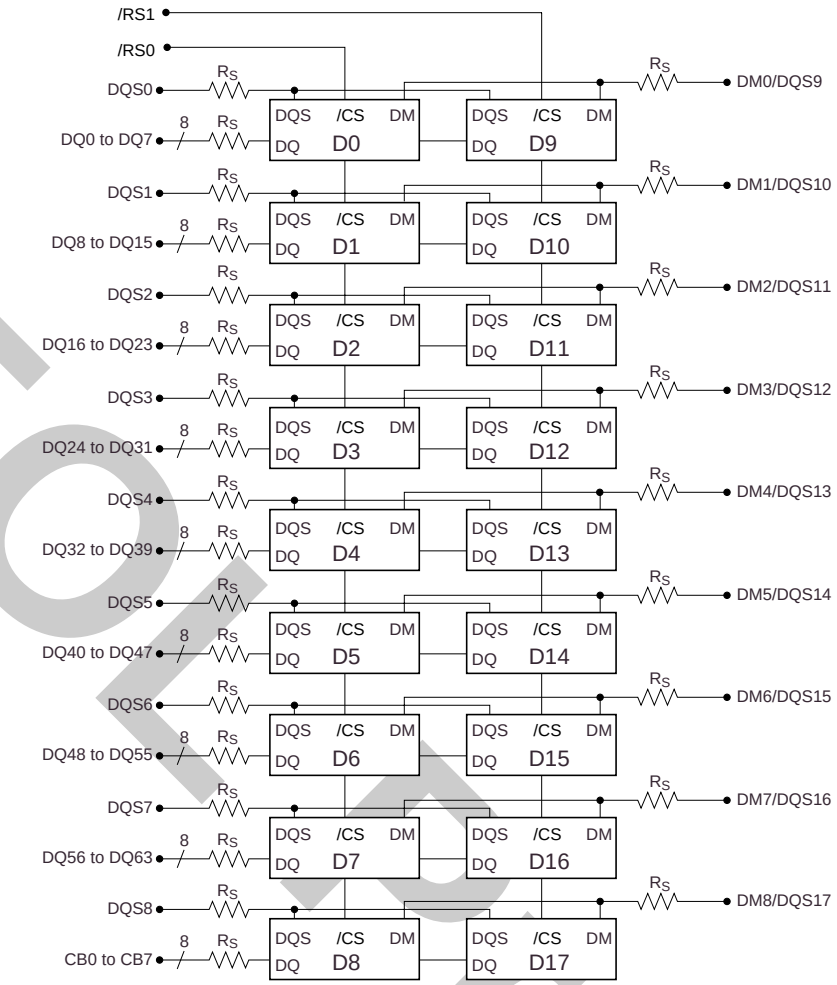
Note: Wire per Clock loading table/Wiring diagrams.

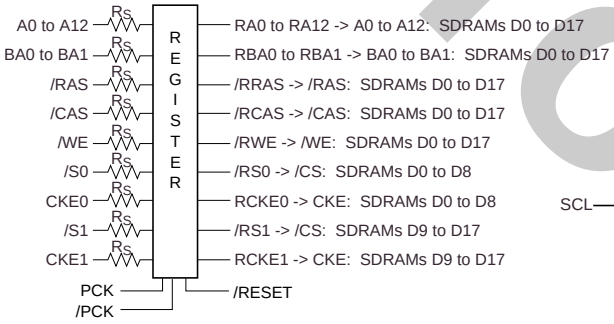
* D0 to D8: HM5425801
U0: 2k-bits EEPROM
R_S: 22Ω
PLL: CDCV857
Register: SSTV16857



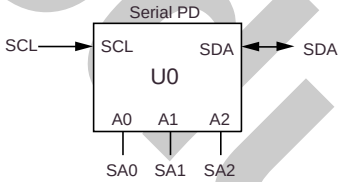
Notes:
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

Block Diagram (HB54A5129F2)

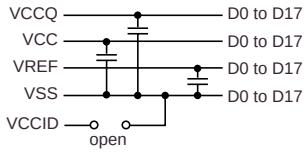




* D0 to D17: HM5425801
U0: 2k bits EEPROM
R_S: 22Ω
PLL: CDCV857
Register: SSTV16857
/RS0 and /RS1 alternate between the back and front side of the DIMM.

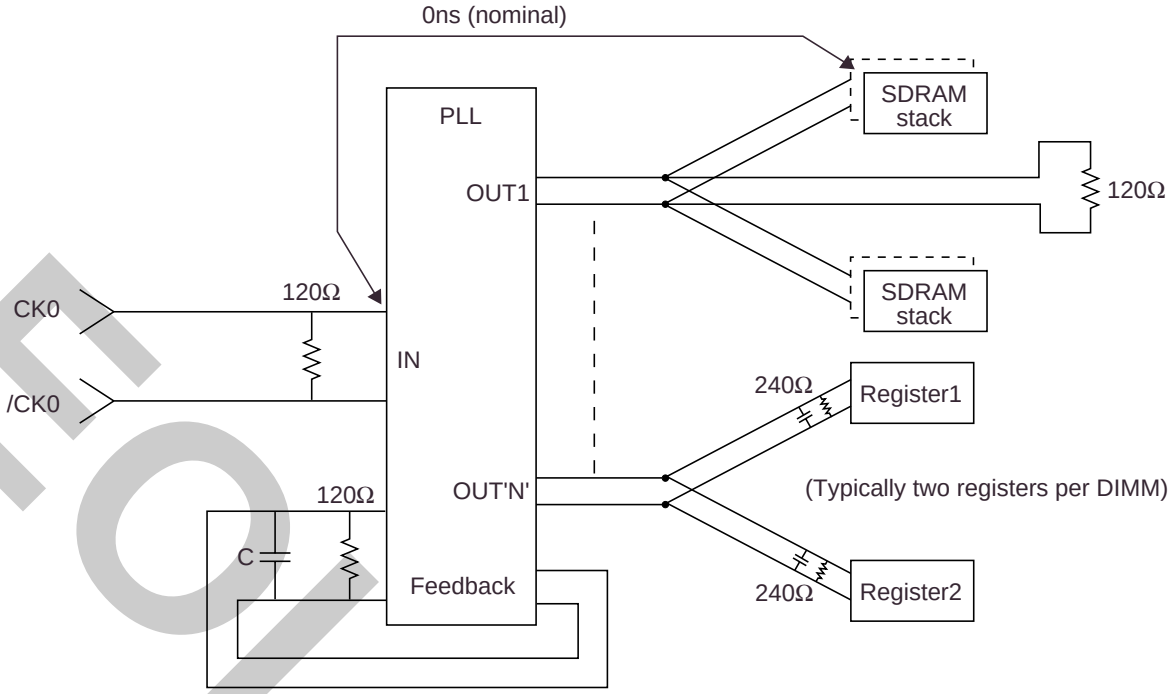


Notes:
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.



CK0, /CK0 ——— PLL*
Note: Wire per Clock loading table/Wiring diagrams.

Differential Clock Net Wiring (CK0, /CK0)



Notes: 1. The clock delay from the input of the PLL clock to the input of any SDRAM or register willl be set to 0 ns (nominal).
2. Input, output and feedback clock lines are terminated from line to line as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
4. Termination resistors for feedback path clocks are located after the pins of the PLL.

Pin Functions (1)

CK (CLK), /CK (/CLK) (input pin): The CK and the /CK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the VREF level. When a read operation, DQSs and DQs are referred to the cross point of the CK and the /CK. When a write operation, DMs and DQs are referred to the cross point of the DQS and the VREF level. DQSs for write operation are referred to the cross point of the CK and the /CK.

/S (/CS) (input pin): When /S is Low, commands and data can be input. When /S is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS, and /WE (input pins): These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A12 (input pins): Row address (AX0 to AX12) is determined by the A0 to the A12 level at the cross point of the CK rising edge and the VREF level in a bank active command cycle. Column address (AY0 to AY9) is loaded via the A0 to the A9, the A11 at the cross point of the CK rising edge and the VREF level in a read or a write command cycle. This column address becomes the starting address of a burst operation.

A10 (AP) (input pin): A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = High when a precharge command is issued, all banks are precharged. If A10 = Low when a precharge command is issued, only the bank that is selected by BA1, BA0 is precharged. If A10 = High when read or write command, auto-precharge function is enabled. While A10 = Low, auto-precharge function is disabled.

BA0, BA1 (input pin): BA0/BA1 are bank select signals. The memory array is divided into bank 0, bank 1, bank 2 and bank 3. If BA1 = Low and BA0 = Low, bank 0 is selected. If BA1 = High and BA0 = Low, bank 1 is selected. If BA1 = Low and BA0 = High, bank 2 is selected. If BA1 = High and BA0 = High, bank 3 is selected.

CKE (input pin): CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven Low and exited when it resumes to High.

The CKE level must be kept for 1 CK cycle (= LCKEPW) at least, that is, if CKE changes at the cross point of the CK rising edge and the VREF level with proper setup time tIS, at the next CK rising edge CKE level must be kept with proper hold time tIH.

Pin Functions (2)

DM (input pins): DM is the reference signals of the data input mask function. DMs are sampled at the cross point of DQS and VREF.

DQ, CB (input and output pins): Data are input to and output from these pins.

DQS (input and output pin): DQS provide the read data strobes (as output) and the write data strobes (as input).

VCC and VCCQ (power supply pins): 2.5V is applied. (VCC is for the internal circuit and VCCQ is for the output buffer.)

VCCSPD (power supply pin): 2.5V is applied (For serial EEPROM).

VSS (power supply pin): Ground is connected.

/RESET (input pin): LVCMOS reset input. When /RESET is low, all registers are reset and all outputs are low.

Detailed Operation Part, AC Characteristics and Timing Waveforms

Refer to the HM5425161B/HM5425801B/HM5425401B Series datasheet (E0086H). DIMM /CAS latency = Device CL + 1 for registered type.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to VSS	VT	–1.0 to +4.6	V	1
Supply voltage relative to VSS	VCC, VCCQ	–1.0 to +4.6	V	1
Short circuit output current	IOUT	50	mA	
Power dissipation	PT	9	W	
Operating temperature	Topr	0 to +55	°C	
Storage temperature	Tstg	–50 to +100	°C	

Notes: 1. Respect to VSS.

DC Operating Conditions (TA = 0 to +55°C)

Parameter	Symbol	min.	Typ	max.	Unit	Notes
Supply voltage	VCC, VCCQ	2.3	2.5	2.7	V	1, 2
	VSS	0	0	0	V	
Input reference voltage	VREF	1.15	1.25	1.35	V	1
Termination voltage	VTT	VREF – 0.04	VREF	VREF + 0.04	V	1
DC Input high voltage	VIH	VREF + 0.18	—	VCCQ + 0.3	V	1, 3
DC Input low voltage	VIL	–0.3	—	VREF – 0.18	V	1, 4
DC Input signal voltage	VIN (dc)	–0.3	—	VCCQ + 0.3	V	5
DC differential input voltage	VSWING (dc)	0.36	—	VCCQ + 0.6	V	6

Notes: 1. All parameters are referred to VSS, when measured.
2. VCCQ must be lower than or equal to VCC.
3. VIH is allowed to exceed VCC up to 4.6V for the period shorter than or equal to 5ns.
4. VIL is allowed to outreach below VSS down to –1.0V for the period shorter than or equal to 5ns.
5. VIN (dc) specifies the allowable dc execution of each differential input.
6. VSWING (dc) specifies the input differential voltage required for switching.

DC Characteristics 1 (TA = 0 to 55°C, VCC, VCCQ = 2.5V ± 0.2V, VSS = 0V)

			HB54A2569F1	HB54A5129F2			
Parameter	Symbol	Grade	max.	max.	Unit	Test condition	Notes
Operating current (ACTV-PRE)	ICC0	-A75B -B75B -10B	1294 1241 1099	1744 1646 1459	mA	CKE ≥ VIH, tRC = min.	1, 2, 5
Operating current (ACTV-READ-PRE)	ICC1	-A75B -B75B -10B	1789 1691 1549	2239 2096 1909	mA	CKE ≥ VIH, BL = 2, CL = 3.5, tRC = min.	1, 2, 5
Idle power down standby current	ICC2P	-A75B -B75B -10B	556 521 487	718 656 595	mA	CKE ≤ VIL	4
Idle standby current	ICC2N	-A75B -B75B -10B	754 701 649	1114 1016 919	mA	CKE ≥ VIH, /CS ≥ VIH	4
Active power down standby current	ICC3P	-A75B -B75B -10B	619 556 514	844 746 649	mA	CKE ≤ VIL	3
Active standby current	ICC3N	-A75B -B75B -10B	844 791 739	1294 1196 1099	mA	CKE ≥ VIH, /CS ≥ VIH tRAS = max.	3
Operating current (Burst read operation)	ICC4R	-A75B -B75B -10B	2419 2321 2224	2869 2726 2584	mA	CKE ≥ VIH, BL = 2, CL = 3.5	1, 2, 5, 6
Operating current (Burst write operation)	ICC4W	-A75B -B75B -10B	2239 2141 2044	2689 2546 2404	mA	CKE ≥ VIH, BL = 2, CL = 3.5	1, 2, 5, 6
Auto refresh current	ICC5	-A75B -B75B -10B	2239 2186 1999	2689 2591 2359	mA	tRFC = min., Input ≤ VIL or ≥ VIH	
Self refresh current	ICC6	-A75B -B75B -10B	421 413 406	448 440 433	mA	Input ≥ VCC – 0.2V Input ≤ 0.2V.	

Notes. 1. These ICC data are measured under condition that DQ pins are not connected.
2. One bank operation.
3. One bank active.
4. All banks idle.
5. Command/Address transition once per one cycle.
6. Data/Data mask transition twice per one cycle.
7. The ICC data on this table are measured with regard to tCK = min. in general.

DC Characteristics 2 (TA = 0 to 55°C, VCC, VCCQ = 2.5V ± 0.2V, VSS = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Notes
Input leakage current	ILI	–10	10	µA	VCC ≥ VIN ≥ VSS	
Output leakage current	ILO	–10	10	µA	VCC ≥ VOUT ≥ VSS	
Output high voltage	VOH	VTT + 0.76	—	V	IOH (max.) = –15.2mA	
Output low voltage	VOL	—	VTT – 0.76	V	IOL (min.) = 15.2mA	

Pin Capacitance (TA = 25°C, VCC, VCCQ = 2.5V ± 0.2V)

[HB54A2569F1]

Parameter	Symbol	Pins	max.	Unit	Notes
Input capacitance	CI1	Address, /RAS, /CAS, /WE, /S, CKE	10	pF	1, 3
Input capacitance	CI2	CK, /CK	20	pF	1, 3
Data and DQS input/output capacitance	CO	DQ, DQS, CB, DM	15	pF	1, 2, 3

[HB54A5129F2]

Parameter	Symbol	Pins	max.	Unit	Notes
Input capacitance	CI1	Address, /RAS, /CAS, /WE, /S, CKE	10	pF	1, 3
Input capacitance	CI2	CK, /CK	20	pF	1, 3
Data and DQS input/output capacitance	CO	DQ, DQS, CB, DM	20	pF	1, 2, 3

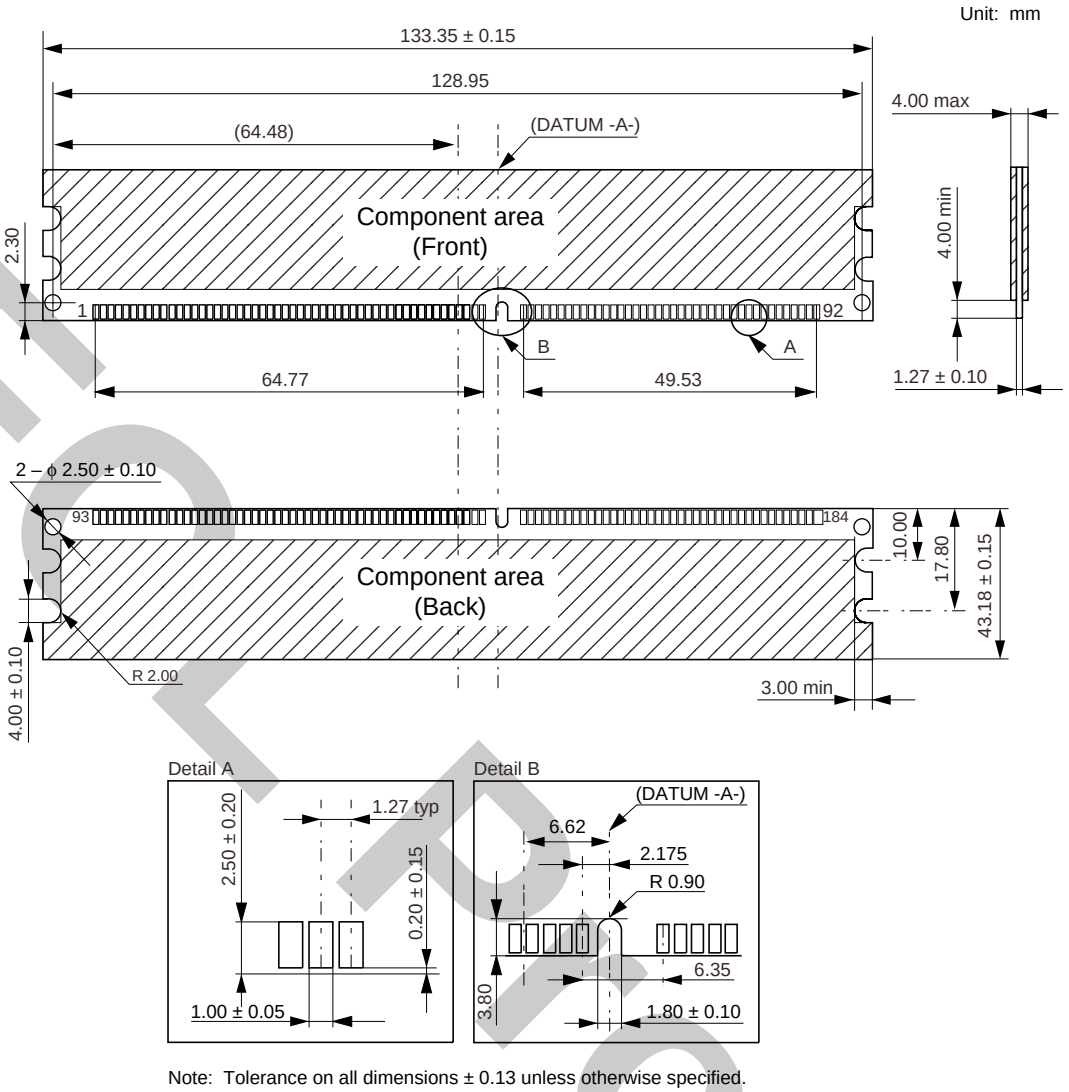
Notes: 1. These parameters are measured on conditions: f = 100MHz, VOUT = VCCQ/2, ΔVOUT = 0.2V.
2. Dout circuits are disabled.
3. This parameter is sampled and not 100% tested.

Timing Parameter Measured in Clock Cycle for Registered DIMM

		Number of clock cycle	
Parameter	Symbol	min.	max.
Write to pre-charge command delay (same bank)	tWPD	3 + BL/2	
Read to pre-charge command delay (same bank)	tRPD	BL/2	
Write to read command delay (to input all data)	tWRD	2 + BL/2	
Burst stop command to write command delay (CL = 3)	tBSTW	2	
(CL = 3.5)	tBSTW	3	
Burst stop command to DQ High-Z (CL = 3)	tBSTZ	3	
(CL = 3.5)	tBSTZ	3.5	
Read command to write command delay (to output all data) (CL = 3)	tRWD	2 + BL/2	
(CL = 3.5)	tRWD	3 + BL/2	
Pre-charge command to High-Z (CL = 3)	tHZP	3	
(CL = 3.5)	tHZP	3.5	
Write command to data in latency	tWCD	2	
Write recovery	tWR	1	
Register set command to active or register set command	tMRD	2	
Self refresh exit to non-read command	tSNR	10	
Self refresh exit to read command	tSRD	200	
Power down entry	tPDEN	1	
Power down exit to command input	tPDEX	1	
CKE minimum pulse width	tCKEPW	1	

Physical Outline

Unit: mm



Note: Tolerance on all dimensions ± 0.13 unless otherwise specified.

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CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.
In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.
Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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